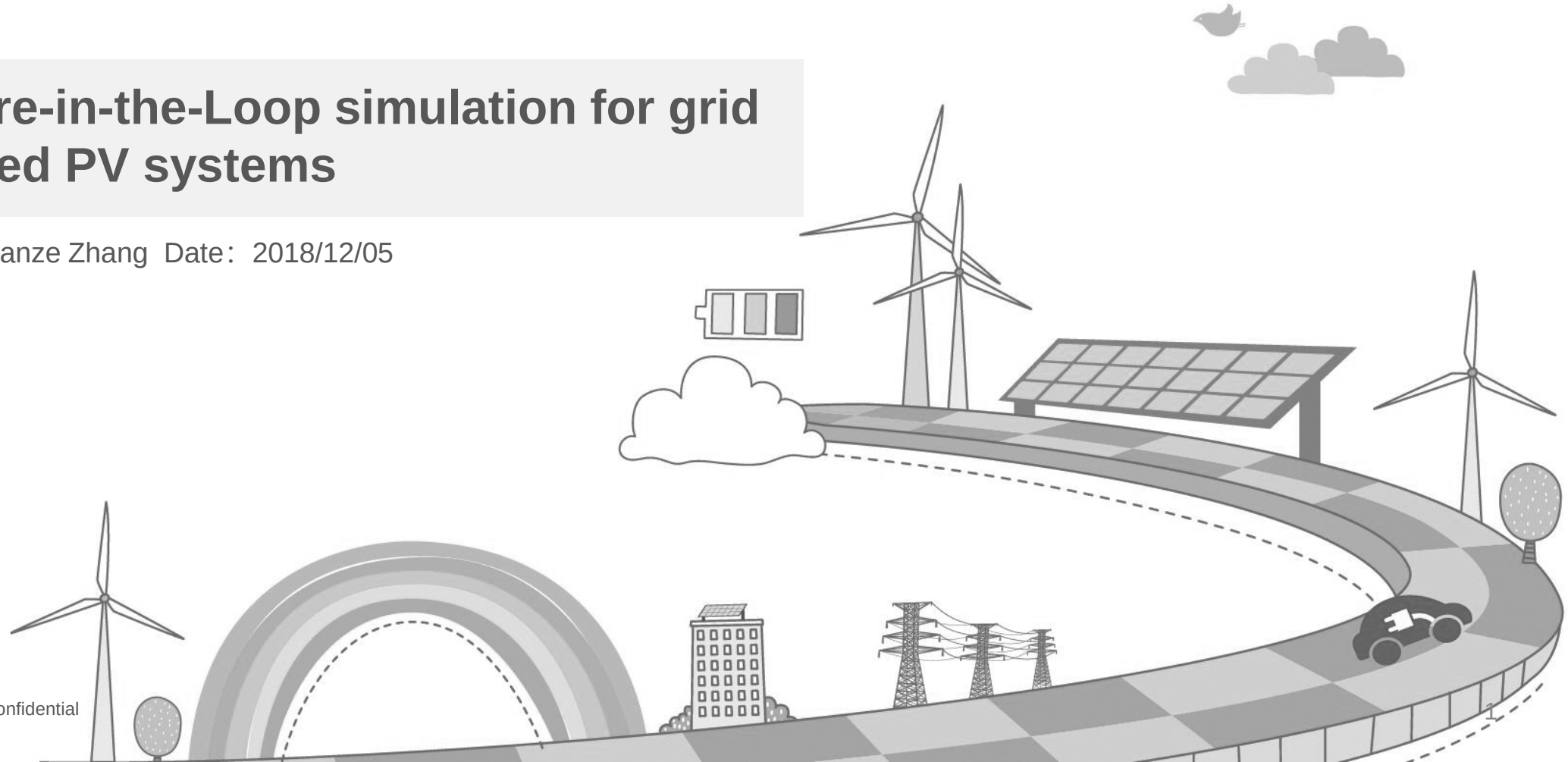
SUNGROW

Clean power for all

Hardware-in-the-Loop simulation for grid integrated PV systems

Reporter：Yuanze Zhang Date：2018/12/05



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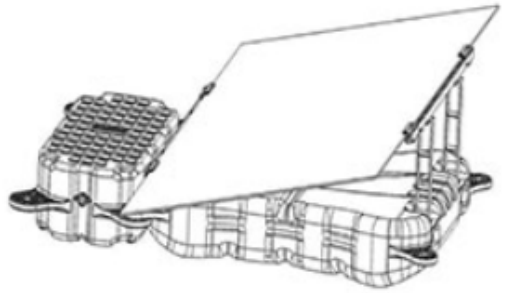
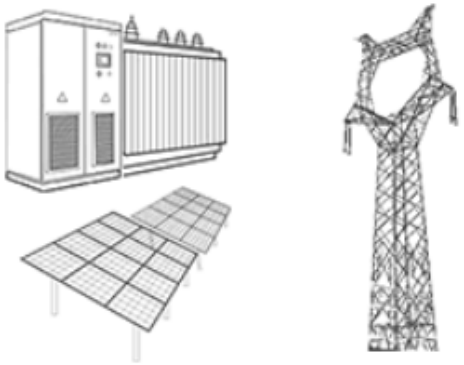
About Sungrow

PV Inverters

Storage System



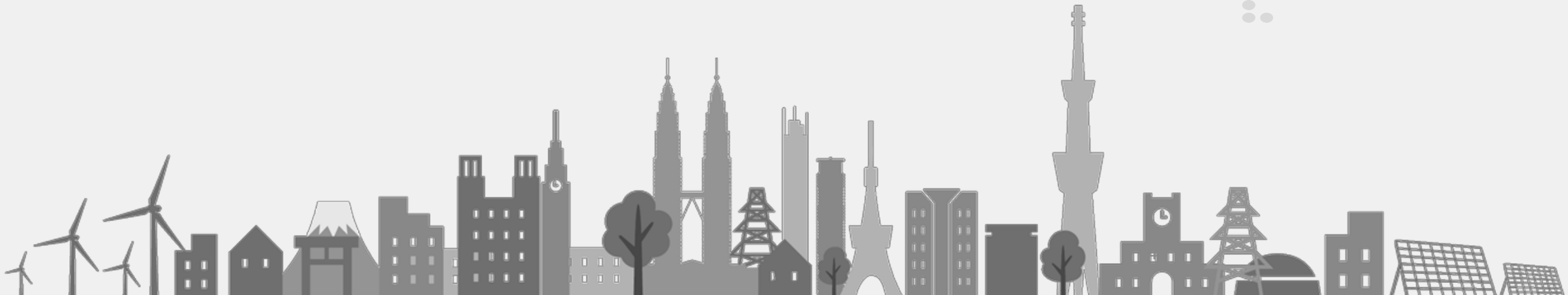
Floating System



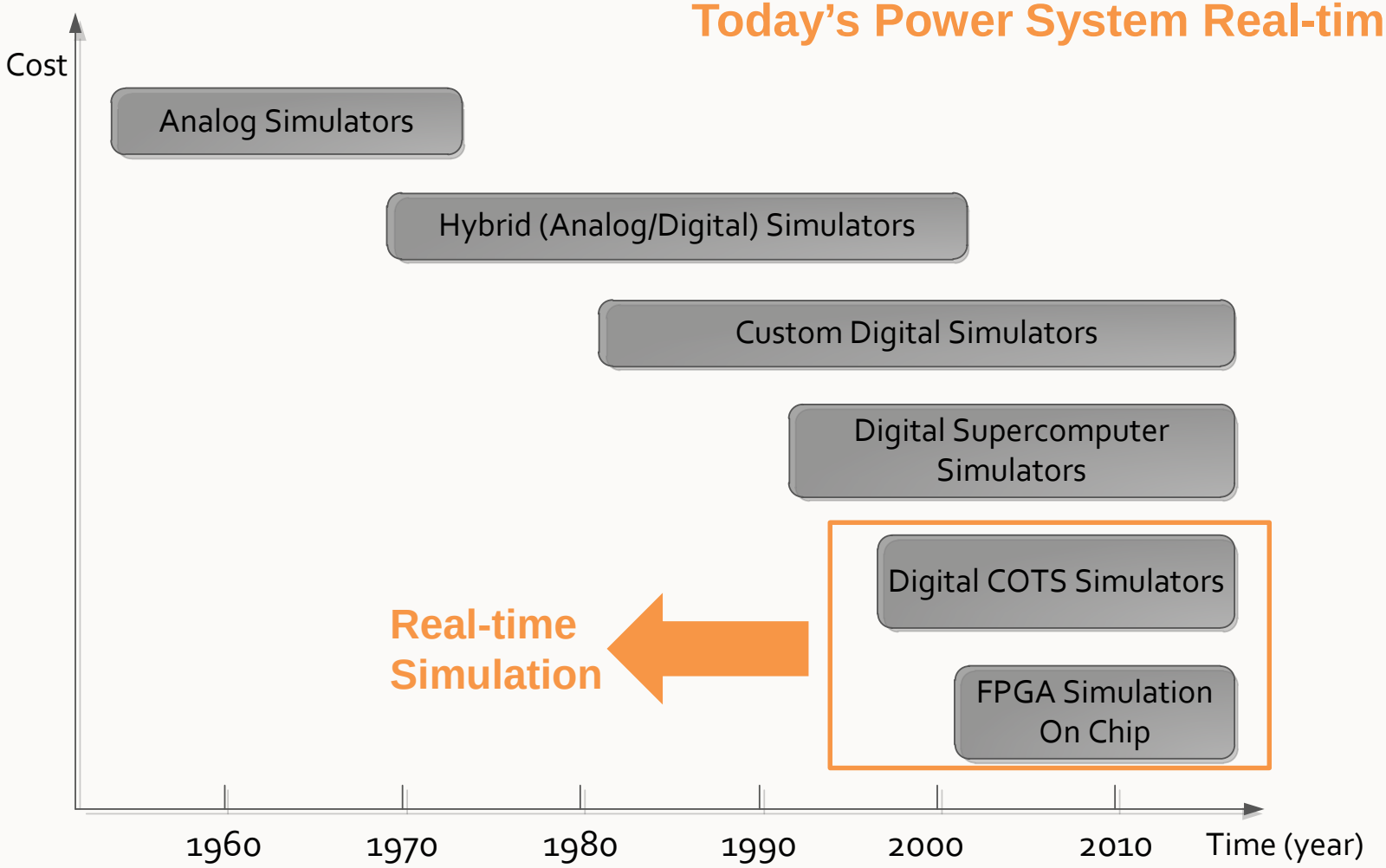
PV Power Plant

Sungrow Power Supply Co., Ltd. is a key high-tech enterprise in China, who specializes in R&D, production, sales, and service of renewable power supply devices for solar energy, wind energy, and energy storage. It's main products include PV inverters, wind converters, energy storage system, electric vehicle drive system, and floaters for floating PV power plants. We also provide first-class solutions for PV power plants.

Real-Time Simulation



A brief history of digital simulators

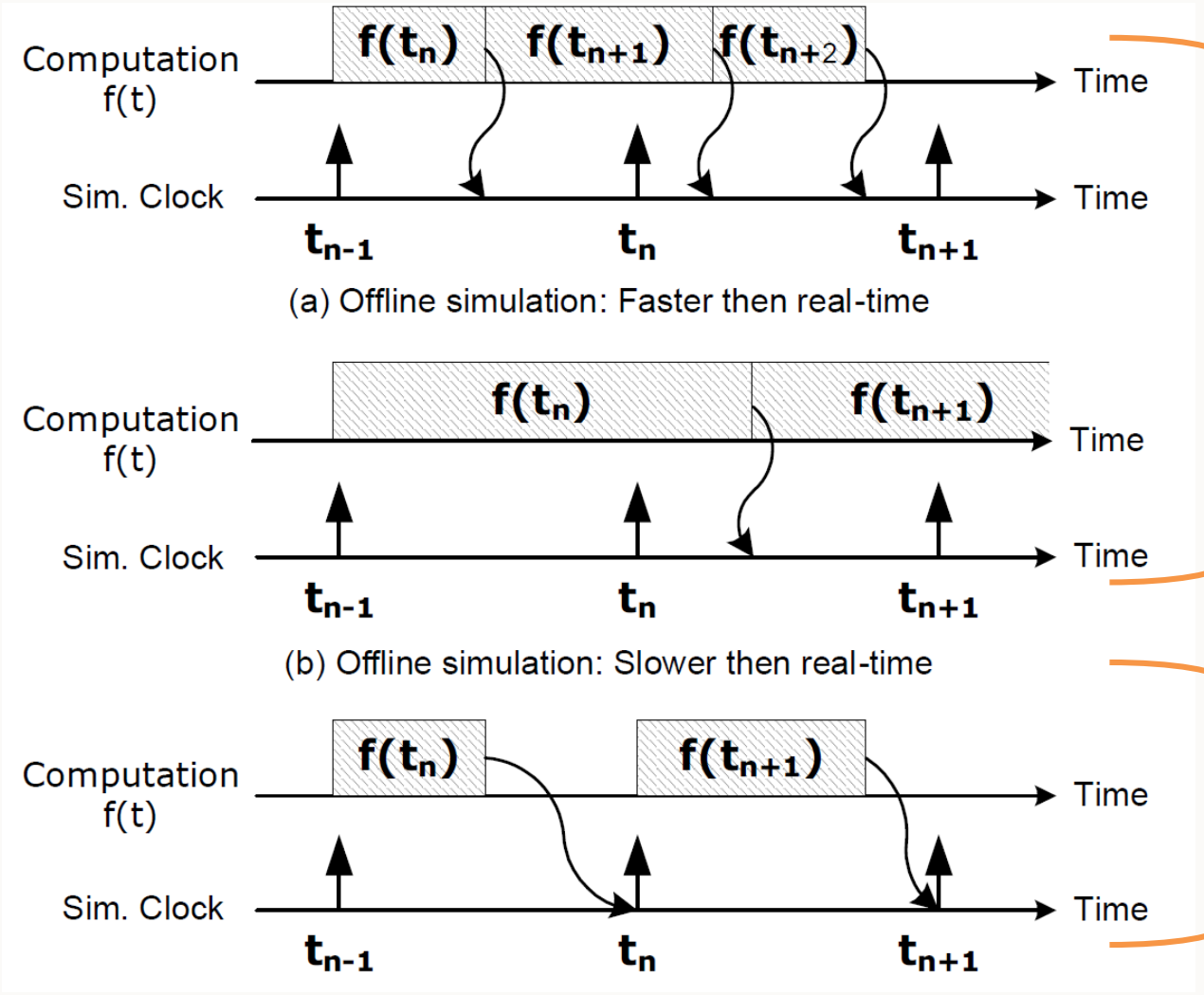


Today's Power System Real-time Simulation requires:

- **High-performance**
- **Scalable**
- **Upgradable**
- **Affordable**

COTS-Based Real-time Digital Simulators

Real-time simulation



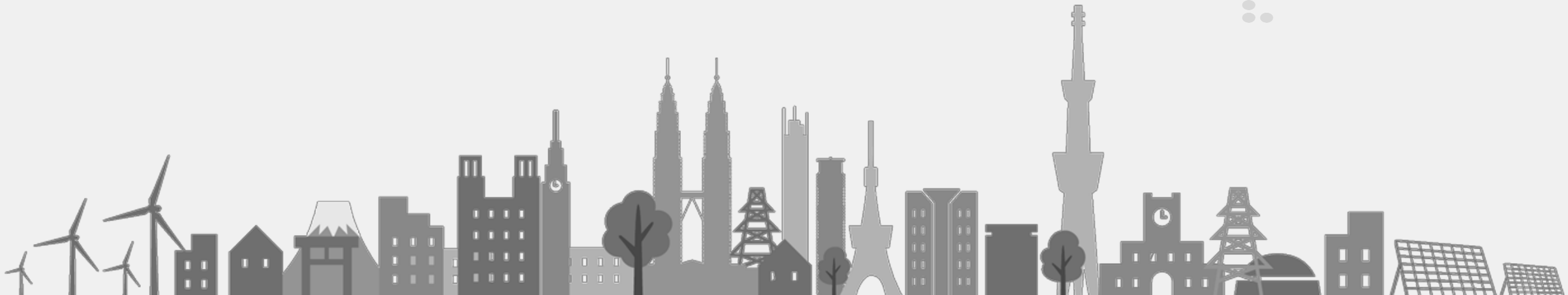
Offline simulation:
Simulation time ≠ wall-clock time
- Faster than real-time Fig. (a)
- Slower than real-time Fig. (b)

Real-time simulation:
Simulation time = wall-clock time
Fig. (c)

Required simulation time < real time: the simulator waits until the clock ticks to the next timestep.

Required simulation time > real time: simulator operations are not all achieved within the required fixed time-step ➡ "overrun".

Hardware-in-the-loop Simulation



Hardware-in-the-loop (HiL) simulation

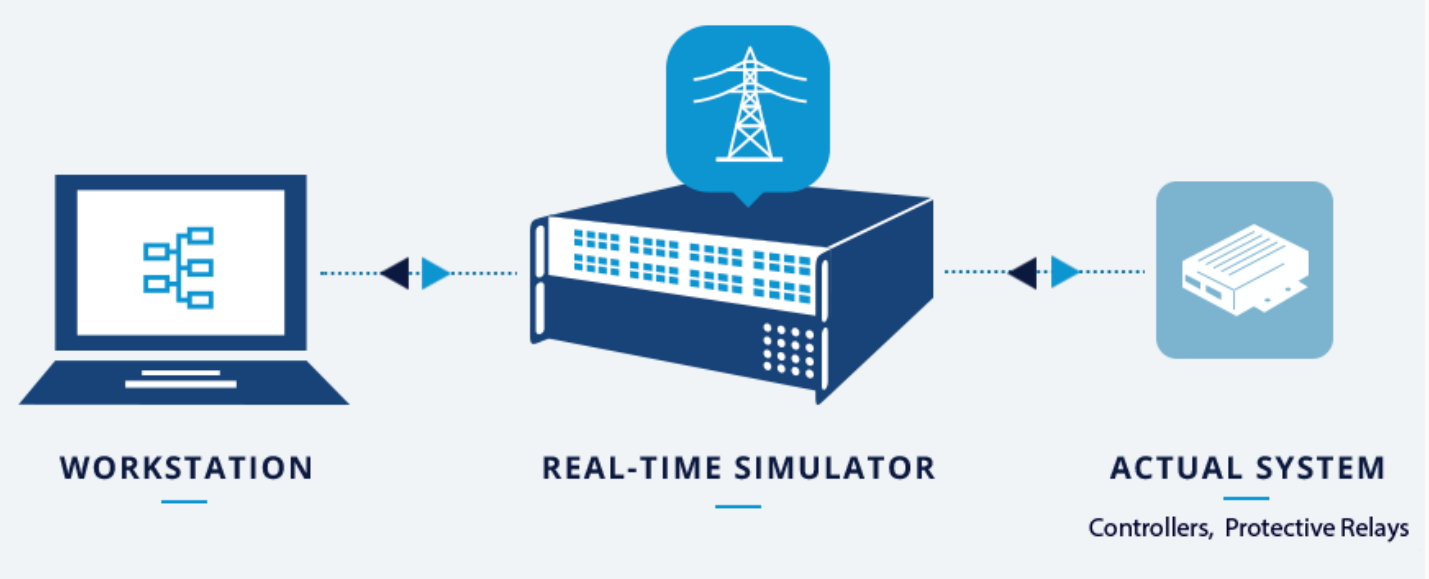
Recently, thanks to the availability of computing power required to simulate power system components and power electronics devices in real-time with the accuracy and precision to represent the transient phenomena, a new method for rapid prototyping and testing control units of power electronics devices, named hardware-in-the-loop (HiL) has emerged.

RTDS Technologies

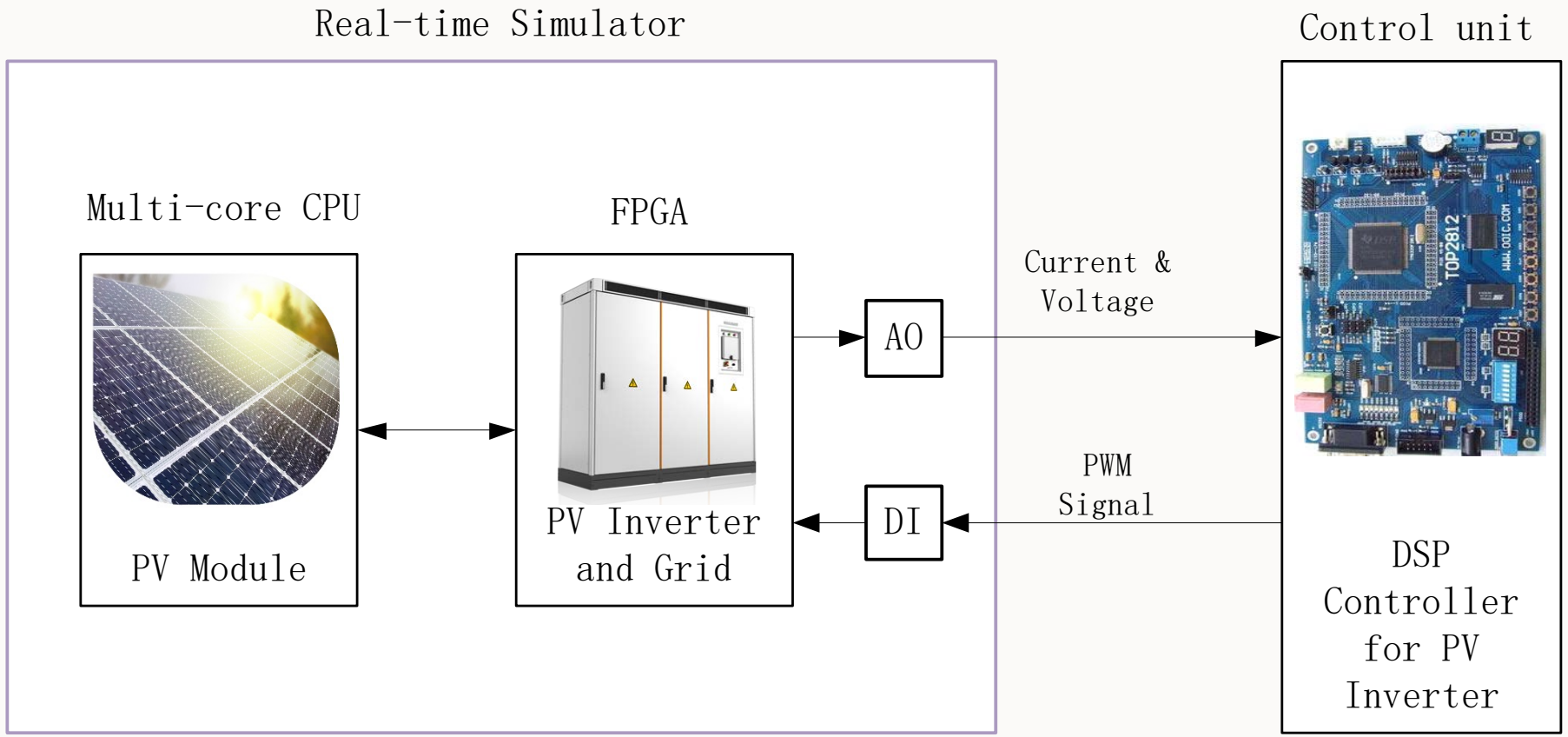
Typhoon HIL

NATIONAL INSTRUMENTS

OPAL-RT TECHNOLOGIES
Electric Drives & Power Electronics HIL Test Benches



Hardware-in-the-loop (HiL) simulation



A HiL simulation system enables users to connect the actual controller to a real-time simulator via input and output (I/O) ports. The PV plants, power electronics devices and power systems are implemented in the simulator as virtual systems, whereas the controller units that connected to the simulator are actual hardware devices.

Benefits of HiL

Save Time

The tight development schedules cannot afford to wait for available prototypes for embedded system testing. By the time a new converter prototype is available for control system testing, as much as 95% of testing will already have been completed using HIL simulation.

Reduce Cost

Frequently, plants are more expensive and have a higher burden-rate than high-fidelity real-time simulators. With few exceptions, developing and testing while connected to a HIL simulator is far more economical than on a physical plant.

Reduce Risk, Increase Safety

HIL simulation enables engineers to perform tests that would otherwise endanger physical plants and the people who work in them. Using HIL, engineers can perform even the most dangerous testing scenarios worry-free, thereby enhancing the safe operation of a plant.

Benefits of HiL

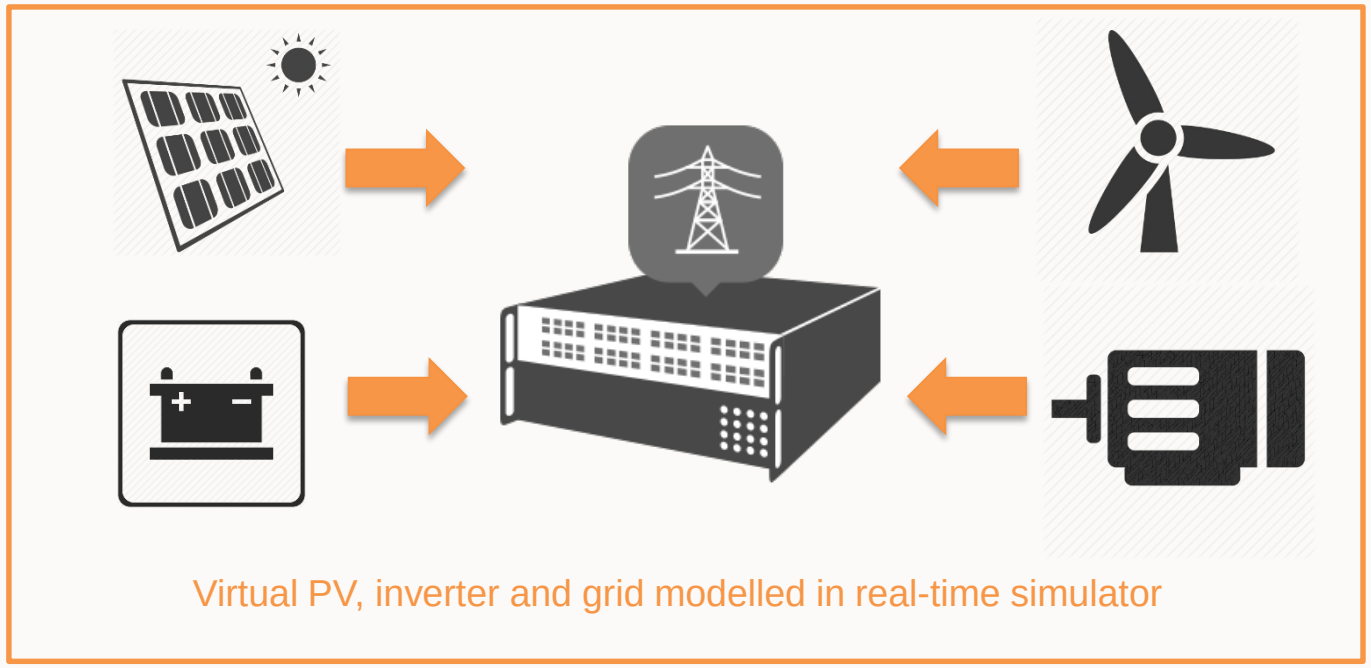
Australia AEMO requirement: Results obtained from off-site tests or factory tests may be used for model confirmation tests. Another approach adopted by power system equipment manufacturers is **Hardware in Loop (HIL)** testing to simulated Disturbances well before plant undergoes on-site commissioning and R2 model validation [1].

IEEE SCC21/P1547.1 Draft Standard Conformance Test Procedures for Equipment Interconnecting Distributed Energy Resources with Electric Power Systems and Associated Interfaces. **HIL testing** is under discussion and likely to be included in the new 1547 standard [2].

The arrival of faster computing capabilities provides a new and unprecedented opportunity for developers. Now, testing time can be significantly reduced. In parallel, design models can be validated and upgraded using **hardware-in-the-loop** data, which are quicker and less expensive to collect than field-based experimental data [3].

What can HiL do?

HiL for power electronics device controller prototyping, testing and tunning:

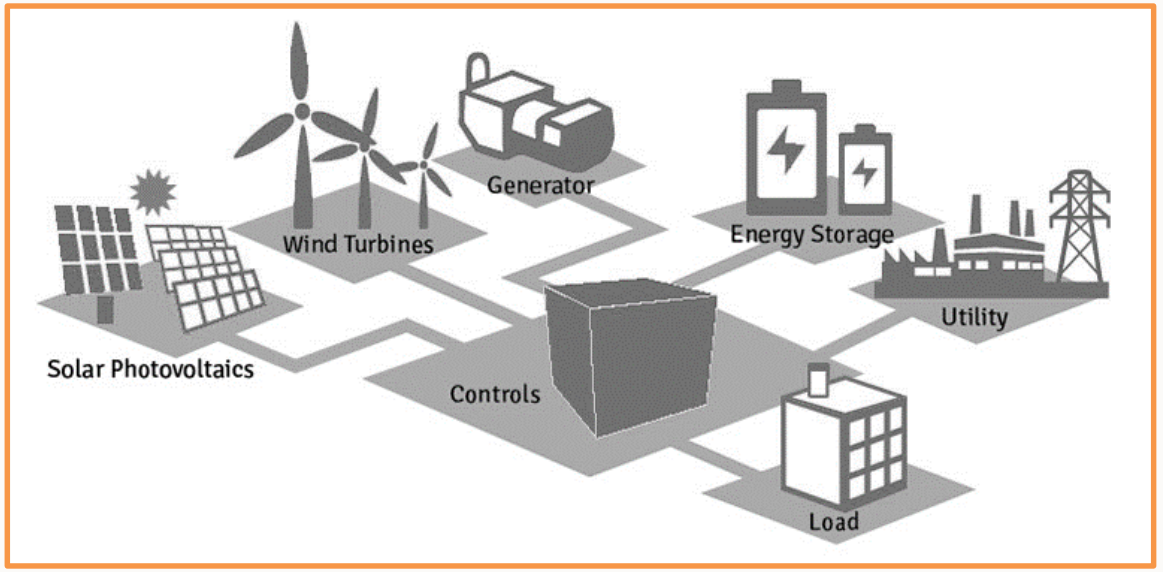


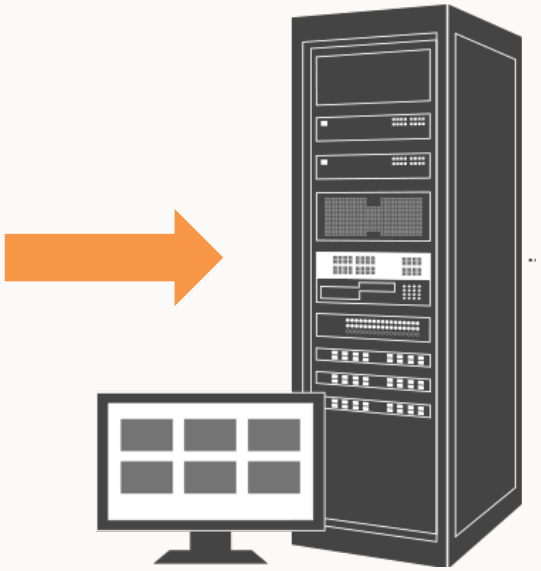
- Support PV source, wind turbine, battery and machine modelling in Matlab/Simulink
- Ideal for fast switching model simulation of power electronics devices
- Capable of real-time fault injection and online parameter adjustment

- Fast control developing
- Control parameter tuning
- Controller performance testing
- Extreme working condition testing

What can HiL do?

HiL for system level simulation





Large-scale plants

Micro-grid

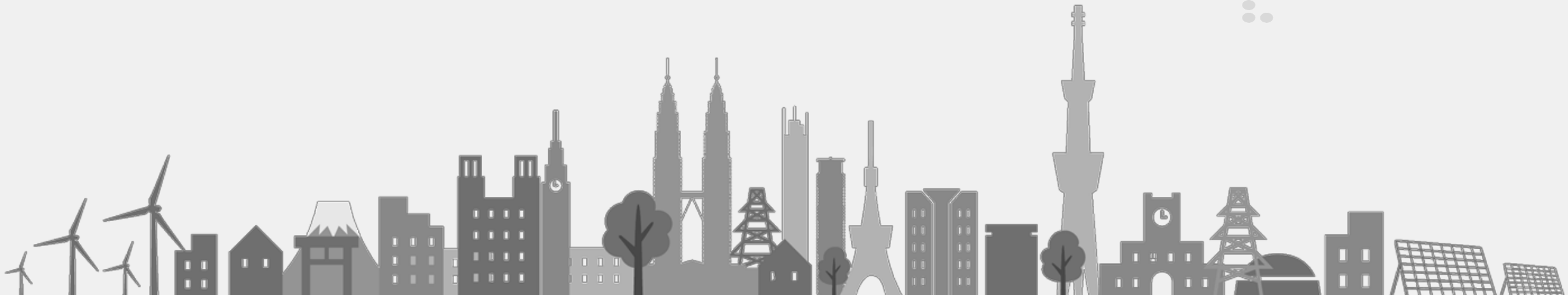
Distributed power generation

HVDC

- Multi-core CPU simulation power
- Support both average and detailed power electronics device modelling
- Precision simulation of controller's characteristic via encapsulation of control algorithm using dynamic linked library.

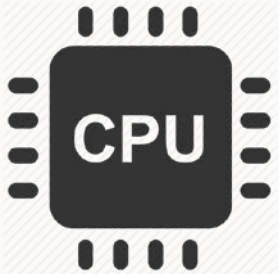
- Enables the realisation of power plant controller (PPC) hardware-in-the-loop simulation
- Ideal for real-time simulation of large scale power plant, micro-grid, distributed generation and HVDC system

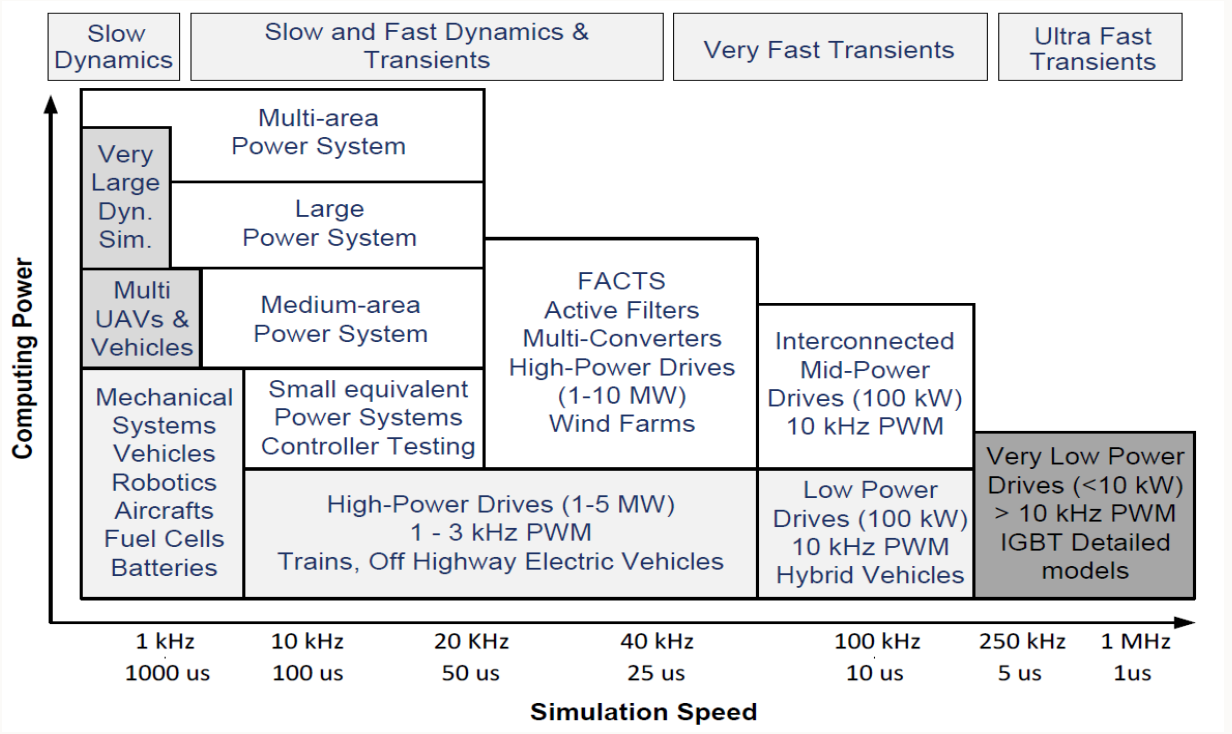
FPGA-Based Simulation

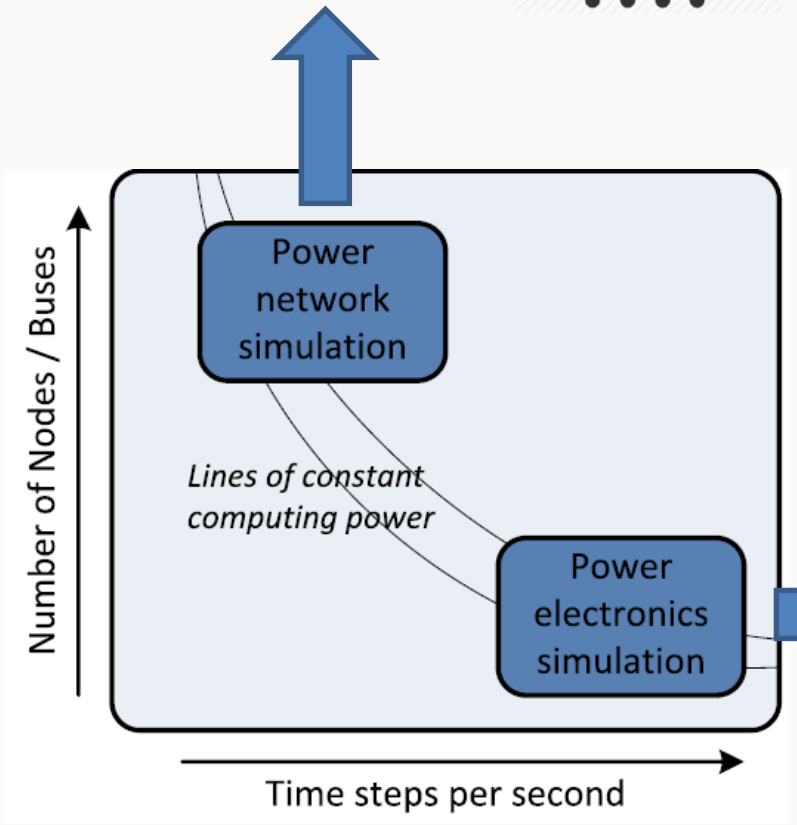


Real-time simulation speed requirement

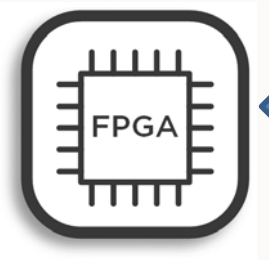
Requires more serial complex computation power



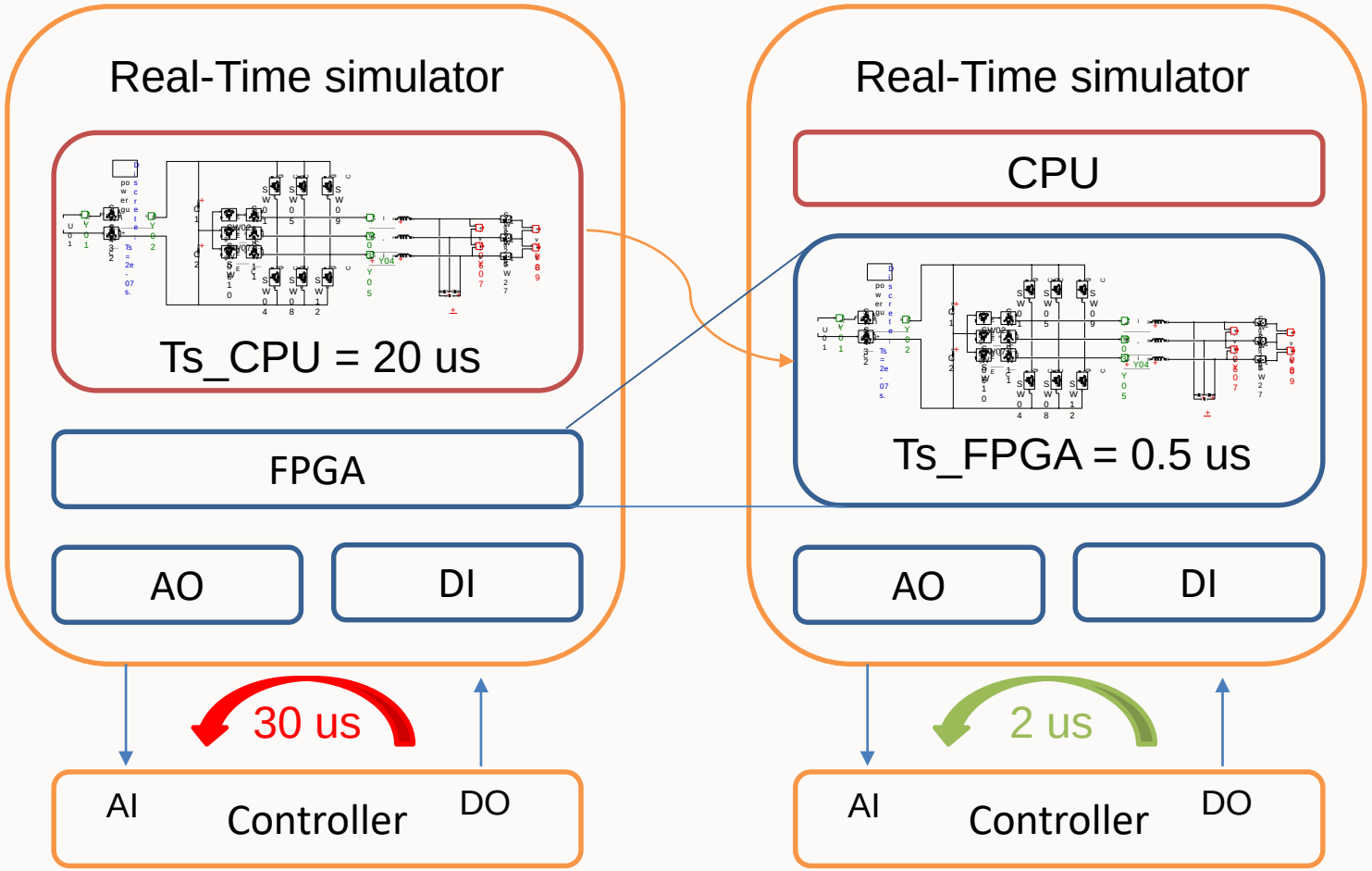




Require simple but parallel fast computation power



FPGA simulation



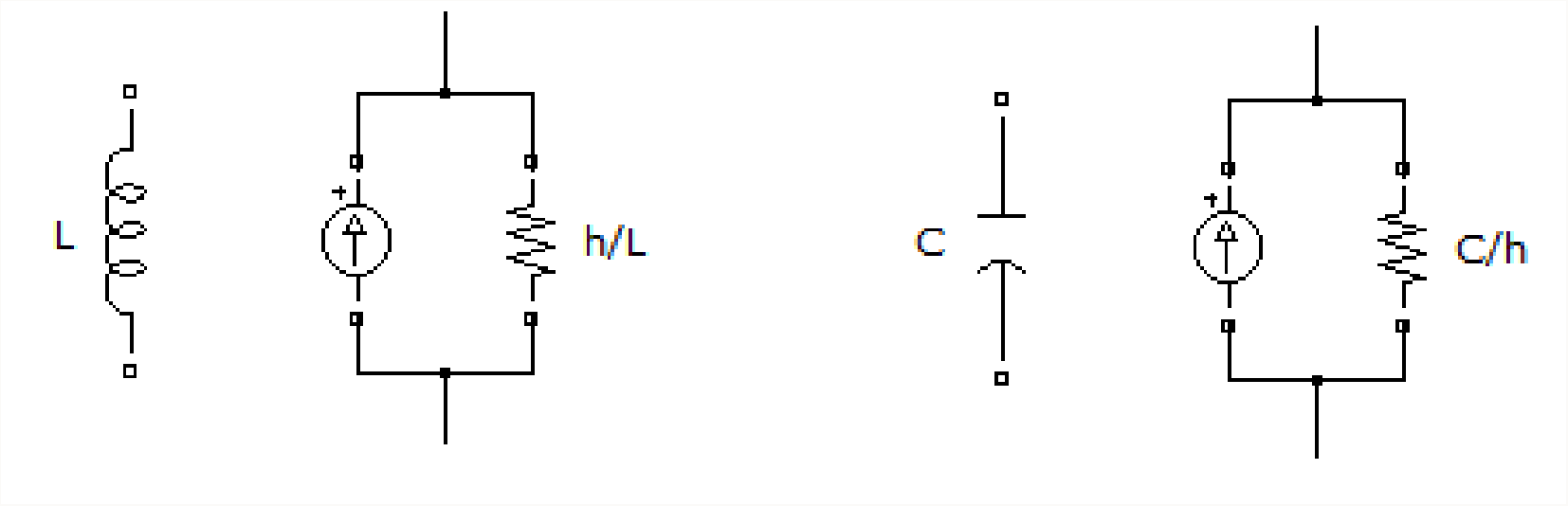
- ❑ CPU Simulation
  - ➢ Minimum simulation step: 20 us
  - ➢ Interface latency: 30 us
  - ➢ Less than 5 kHz switching frequency
- ❑ FPGA Simulation
  - ➢ Minimum simulation step: 0.5 us
  - ➢ Interface latency: 2 us
  - ➢ 10~100 kHz switching frequency

FPGA simulation

Pejovic method

Pejovic method replaces switches by either an inductance when conducting or a capacitor when blocking in the nodal matrix. This method is called the fix-Y because the conductance matrix does not change when a switch changes state.

When using the modified nodal analysis the main difference between an inductance and a capacitor is in their discretization and in their historical term. Once discretised, the equivalent circuit is a current source with a shunt resistance.



FPGA simulation

Pejovic method

For the matrix to remain the same upon switching event, the following equation must remains true

$$Gs = h/L = C/h$$

where h is the time step

When building the nodal matrix a value between 10 and 0.001 has to be set to represent a switch. This determines the value of the inductance and the capacitor representing the switch.

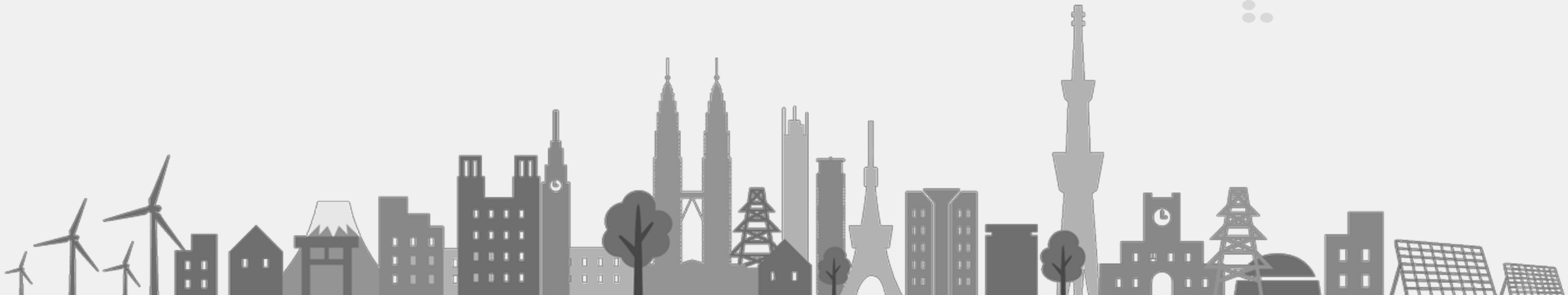
$$L=h/Gs \qquad C=h\times Gs$$

For a time step 100ns and a Gs=1, the switch will be represented by the following inductance and capacitor.

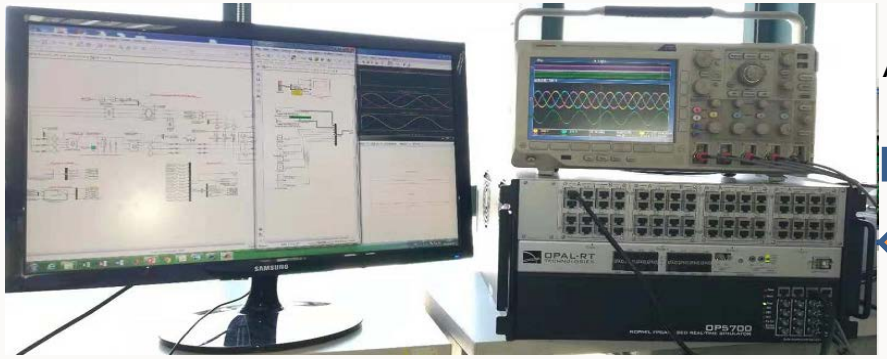
$$L = h/Gs = 100ns/1=100nH$$
$$C=h \times Gs = 100ns\times 1=100nF$$

Ideally, you want to have a very small inductor and a very small capacitor to represent a ideal switch. Depending of the circuit topology you might get better result by choosing a different value of Gs [4].

HiL For Integrated PV Systems

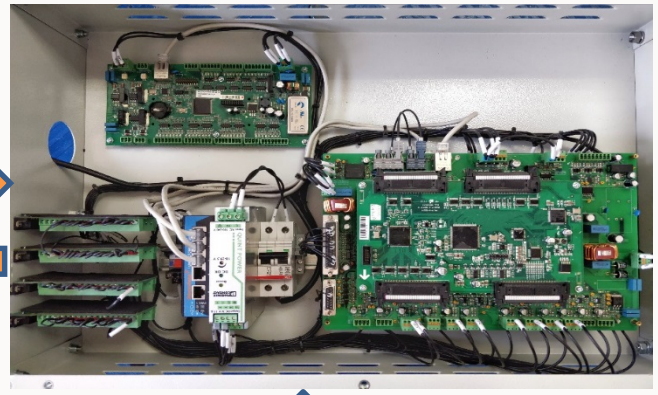


HiL experiment bench setup



Analogue & Digital I/O

PWM



- Inverter Controller
  - Provides embedded inverter control
  - Receive analogue signal
  - Generate PWM gate drive signal

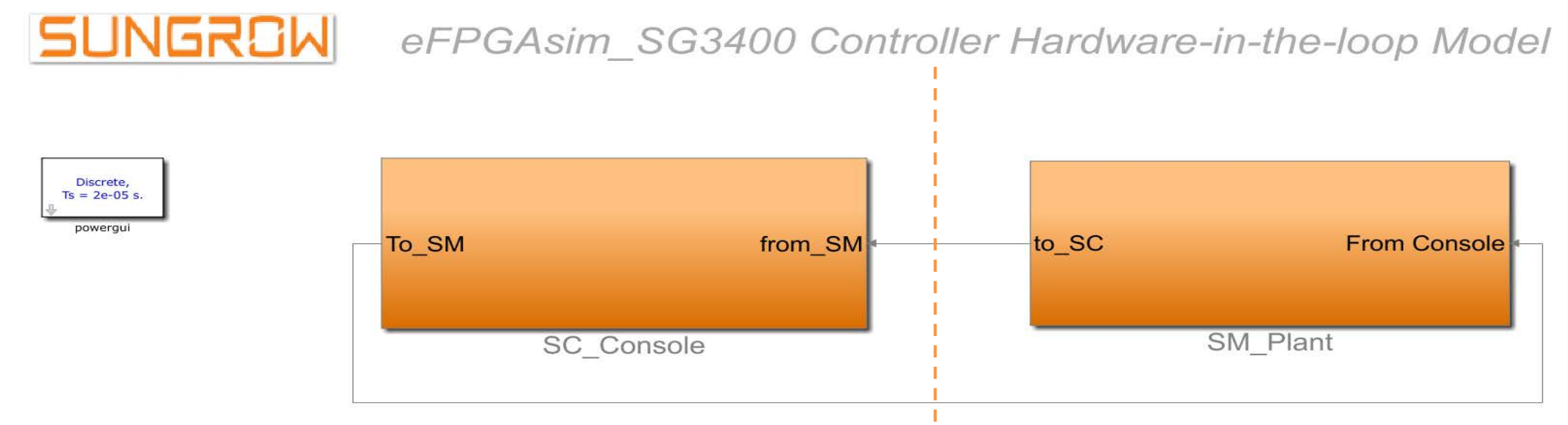
RS485

- Host computer
  - Build simulation model
  - On-line parameter adjusting and fault injection
  - Collect simulation data

- Real-time simulator
  - CPU and FPGA simulation
  - Analog and digital signal IO

- Human & machine interface panel
  - Inverter working condition monitoring
  - Control parameter setting

System model in CPU

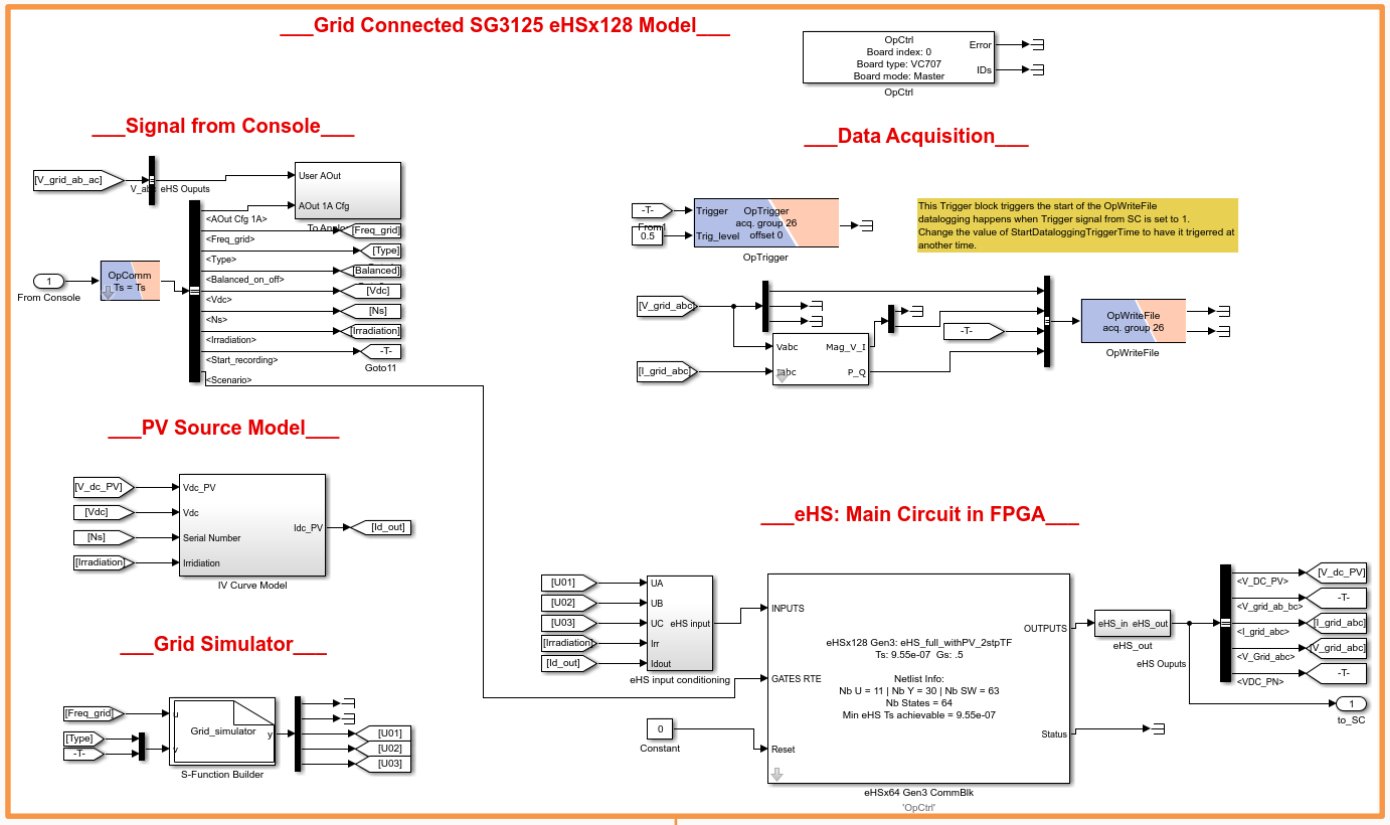


- SC Console Subsystem
  - Allows interaction with the system during execution.
  - Runs on host pc asynchronously from the other subsystems.
  - Not linked to a computation node (core).
  - All user interface blocks (scopes, displays, switches, controls, etc)
  - No signal generation nor important mathematical operations

- SM Master Subsystem
  - Content: All the computational elements of the model, the mathematical operations, the I/O blocks, the signal generators, etc.

System model in CPU

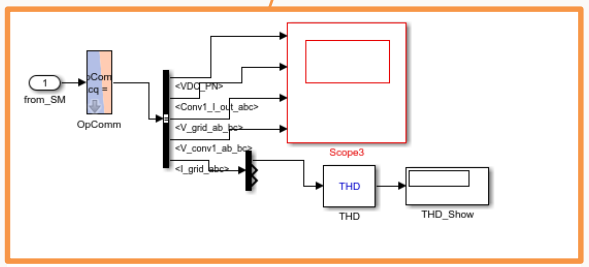
❑ SM Master Subsystem

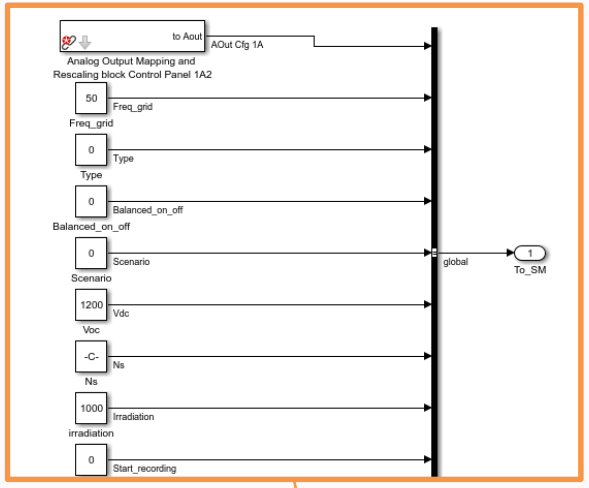


- I/O channel arrangement
- FPGA setting
- Grid simulator
- Data acquisition
- PV source model

SC Console Subsystem

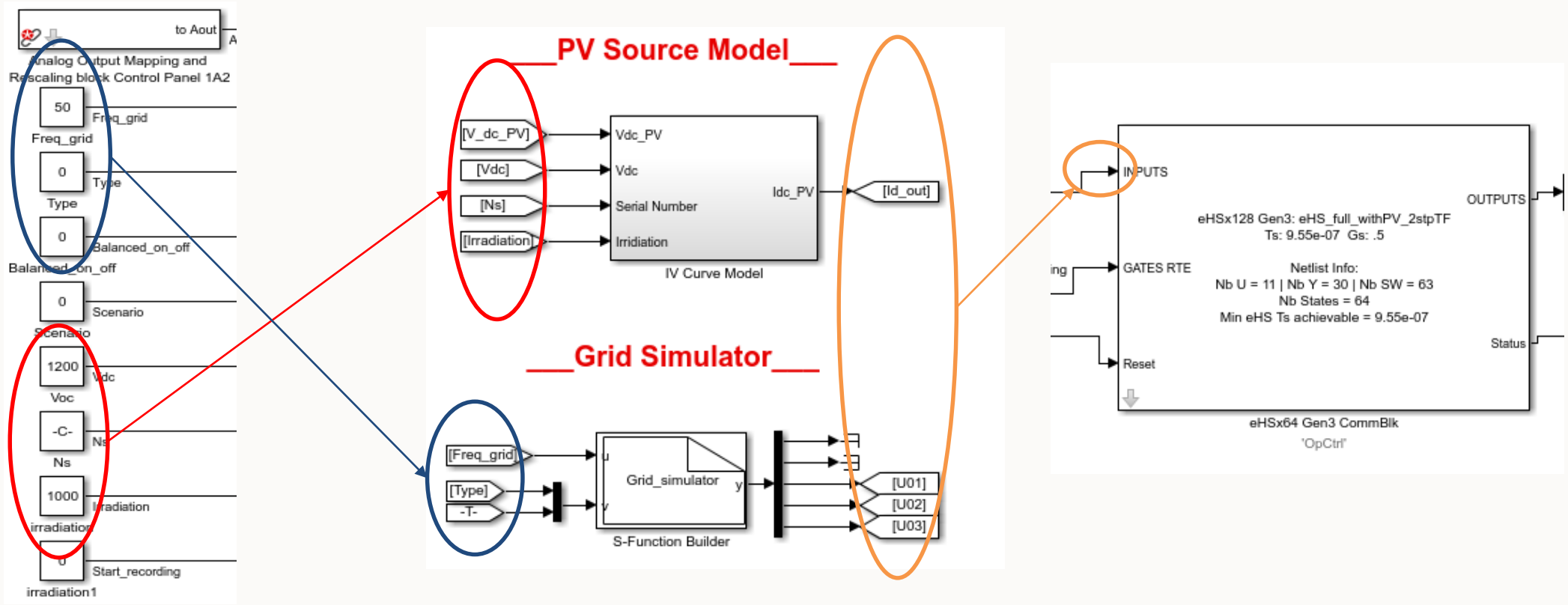
Scopes & measurements





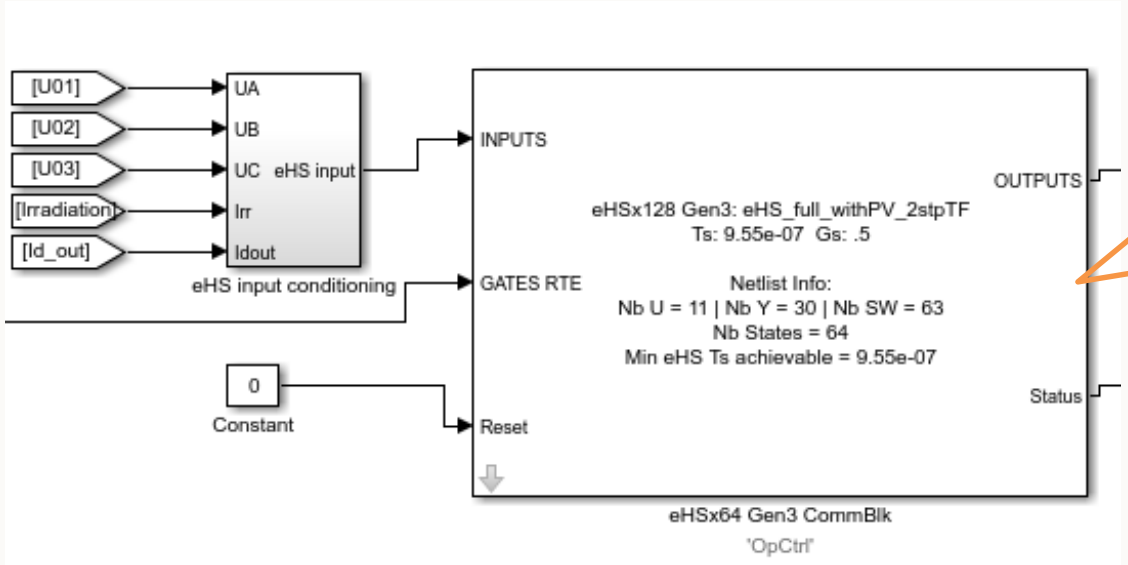
Real-time parameter setting & fault injection

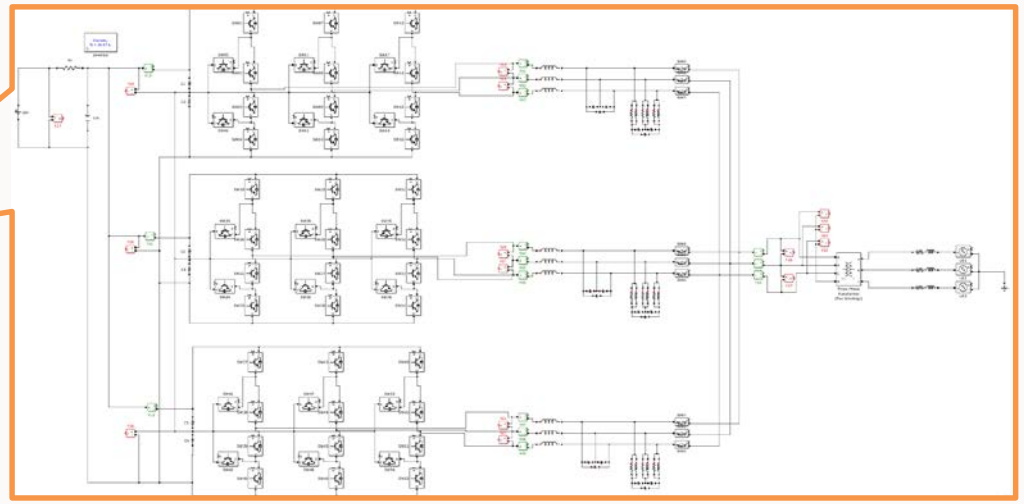
System model in CPU



- Console:
  - Online parameter adjusting
  - Fault injection
- CPU model interface
  -- slow simulation speed:
  - PV Model
  - Grid Model
- FPGA model interface
  -- fast simulation speed:
  - Inverter

Inverter and grid model in FPGA

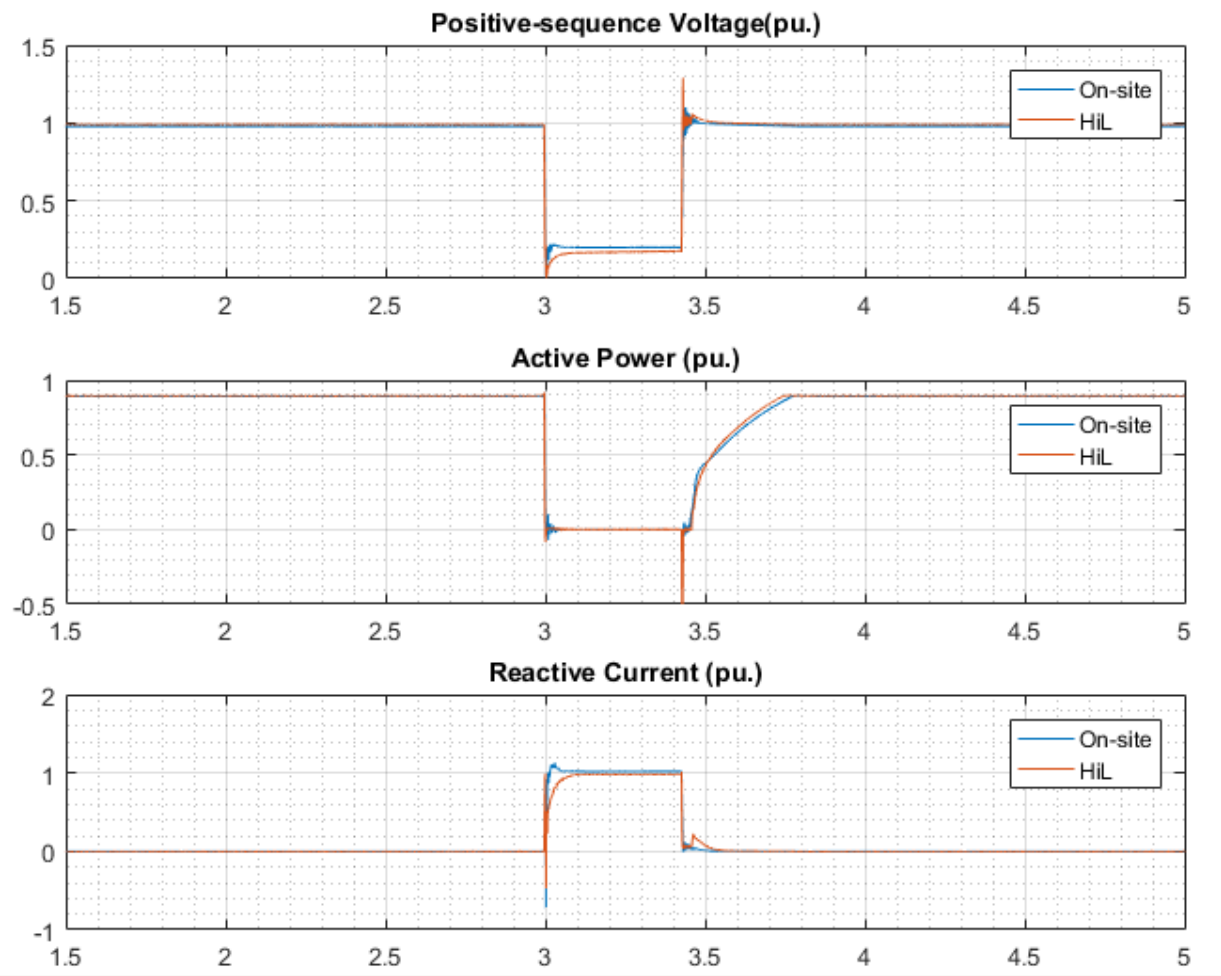




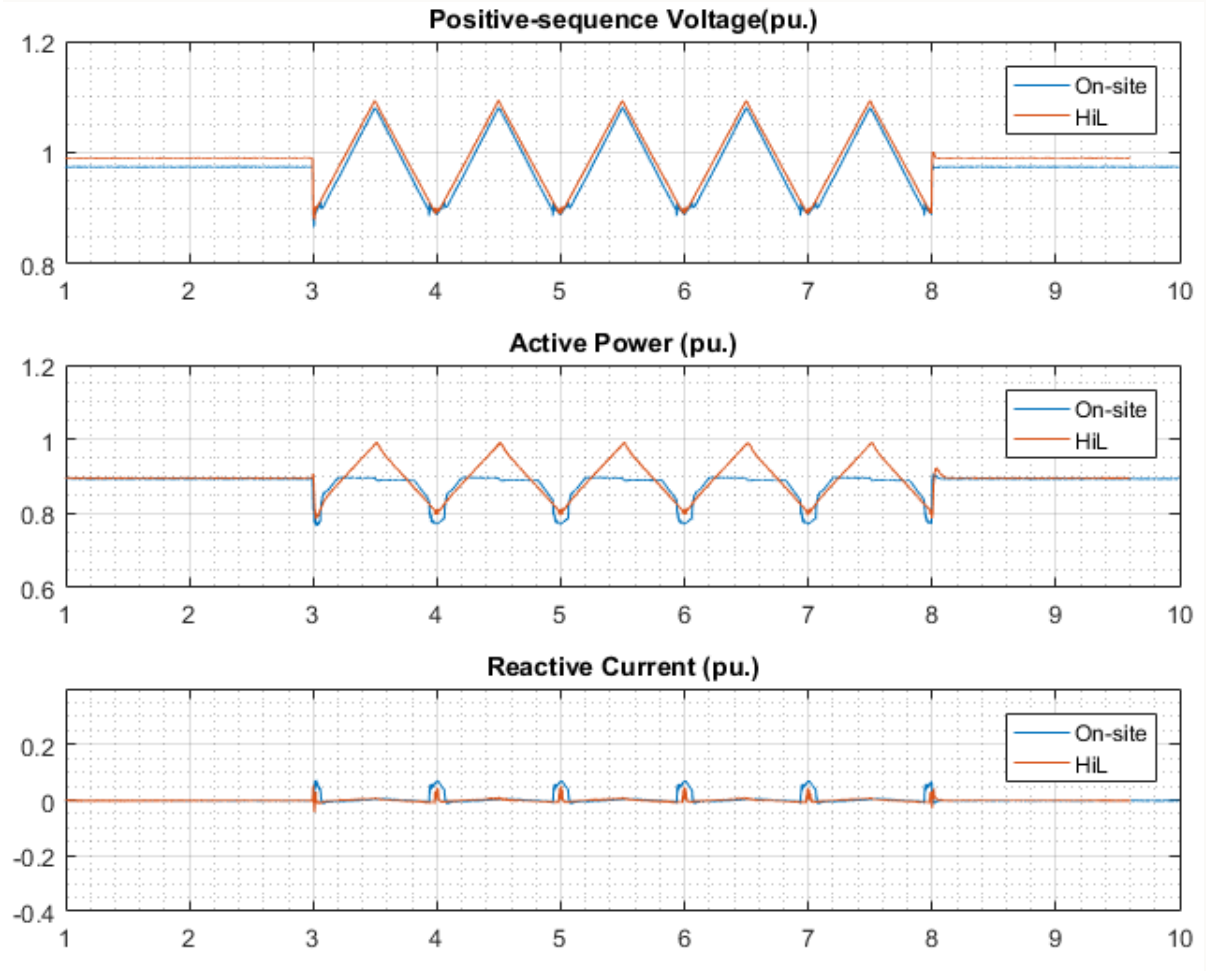
- eHS interface between CPU and FPAG model
  - Arrange PMW channels
  - Set PMW gate properties
  - Determine FPGA simulation steps
  - Channel Input & output of FPGA model
  - Define the value of Gs

- SG3125 there-level IGBT detailed switching model
  - Detailed switching model
  - Fast simulation step: 1us

HiL simulation results

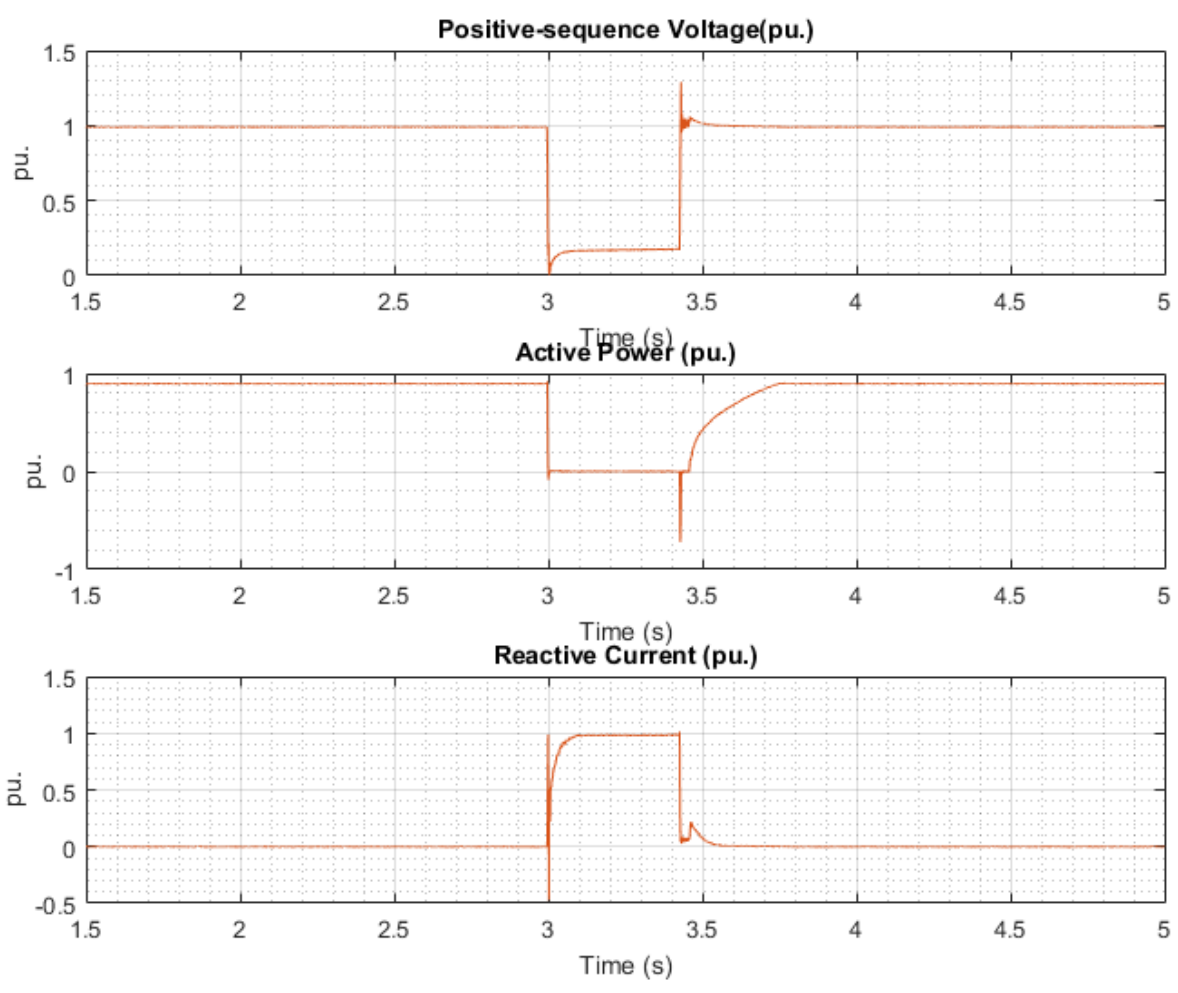


SG3400 LVRT on-site measurement vs. RT-Lab HiL (90% load, 80% dip)

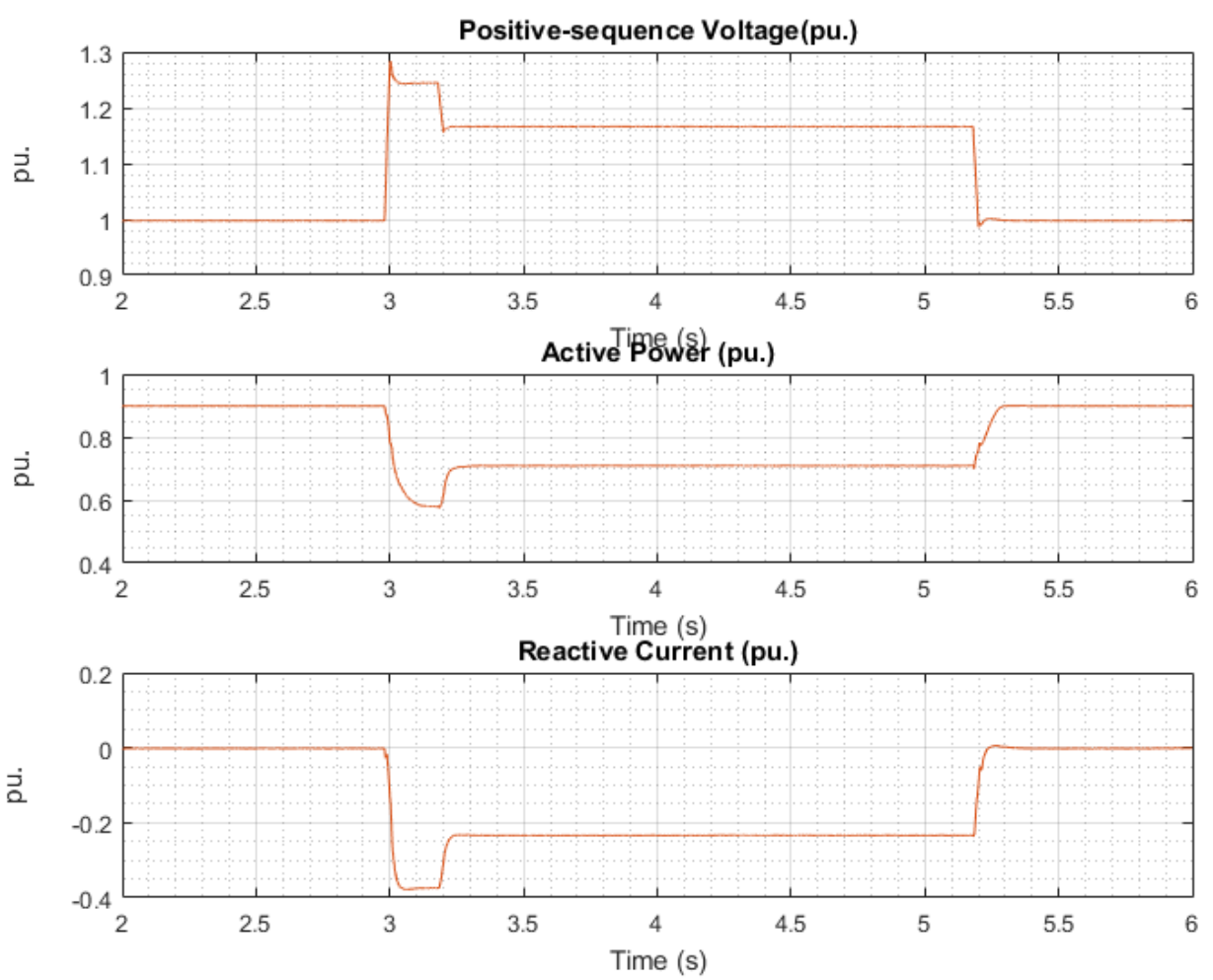


SG3400 POC voltage fluctuation on-site measurement vs. RT-Lab HiL

HiL simulation results



SG3400 LVRT RT-Lab HiL (90% load, 0% dip) SCR = 3



SG3400 HVRT RT-Lab HiL (90% load, 0% dip) SCR = 3

Reference

[1] Power System Model Guidelines, AEMO Mar. 2018, available at: https://www.aemo.com.au/

[2] IEEE SCC21/P1547.1 Draft Standard Conformance Test Procedures for Equipment Interconnecting Distributed Energy Resources with Electric Power Systems and Associated Interfaces, Oct. 2016, available at: http://grouper.ieee.org/groups/scc21/1547.1_revision

[3] Hardware-in-the-Loop Testing of Utility-Scale Wind Turbine Generators, R. Schkoda, C. Fox, and . H. Clemson University, V. Gevorgian, R. Wallen, and S. Lambert, National Renewable Energy Laboratory, available at: https://www.nrel.gov/docs/fy16osti/64787.pdf

[4] eHardware Solver Tutorial, Opal-RT, 2013

THANK YOU!